

APPROVE
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Figure 1 is a plan view of a semiconductor device 20. The device is divided into three vertical sections 15a, 15b, and 15c. Each section contains a series of memory cells 16. The cells are arranged in rows and columns, with word lines (S1, S2, S3, S4) and bit lines (GC1, GC2, GC3, GC4) intersecting. Power supply lines VDD 11 and VSS 12 are shown at the top and bottom. Various components are labeled with numbers 17 through 19 and letters S1 through S8.

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